WHAT IS CLAIMED IS:

1. A method of conserving power in a multiprocessor device including a plurality of PUs (processor units), comprising the steps of:

providing a plurality of blocking channels associated with a like plurality of PUs;

setting a PU to a sleep mode when the channel is blocked for the operation the processor is attempting; and

returning a PU to normal power conditions when a given type of channel event occurs.

2. A method of conserving the use of electrical energy in a computer processor, comprising:

providing a mechanism for blocking transactions; and

placing the processor into a low-power state when a blocked transaction exists.

3. The method of claim 2, wherein the transactions are program instructions and the method comprises the additional steps of:

providing a depository channel for instructions internal to the processor; and

providing a depository blocking channel for instructions external to the processor.

4. The method of claim 2, wherein blockings transactions are channel read or channel write instructions.

5. The method of claim 2, wherein channel state is maintained with a channel (transaction pending) count.

6. The method of claim 2, wherein the processor is reawakened when the environment performs a transaction that removes the block causing the blocked transaction.

7. The method of claim 2, wherein:

the processor is part of a multiprocessor system; and

the blocked transaction is caused in awaiting a response from another processor of the multiprocessor system.

8. A method of conserving the use of electrical energy in a multiprocessor system, comprising:

providing a mechanism for blocking transactions in at least a plurality of processors of the multiprocessor system; and

placing the a processor into a low-power state when a blocked transaction exists.

9. The method of claim 8, wherein the blocking transaction is caused by the awaiting of a response from the environment.

10. The method of claim 9, wherein:

the multiprocessor is on a single chip; and

the environment of a given processor is at least in part on the single chip.

11. The method of claim 9, wherein the environment may include another processor.

12. Apparatus for conserving the use of electrical energy in a processor, comprising:

blocking channel data storage means operable to contain data for use in connection with the environment outside the

processor; and

low power means operable to place the processor in a low power mode while awaiting a response from the environment.

13. Apparatus for conserving the use of electrical energy in a processor, comprising:

blocking channel data storage means operable to contain data for use in connection with the environment outside the processor; and

low power means operable to place the processor in a low power mode when the blocking channel is at least one of full and empty.

14. Apparatus for conserving the use of electrical energy in a processor, comprising:

blocking channel data storage means operable to contain data for use in connection with the environment outside the processor; and

low power means operable to place the processor in a low power mode while awaiting a response from the environment.

15. Apparatus for conserving the use of electrical energy in a processor, comprising:

blocking transaction means;

monitoring means operable to place the processor in a low-power state when a blocked transaction condition is detected.

16. A method of conserving the use of electrical energy in a computer processor, comprising:

normally keeping the processor in a low power state; and

awakening the processor to an active state for only as long as the processor can usefully process data.

17. The method of claim 16, comprising, in addition, activation signals accompanying the issue of instructions to accomplish the awakening of the processor.

18. Apparatus for conserving the use of electrical energy in a computer processor, comprising:

a processor normally maintained in a low power state; and

detection means operable to awaken the processor to an active state for only as long as the detection means ascertains that the processor can usefully process data.

19. The apparatus of claim 18, wherein the detection means is responsive to activation signals accompanying the issue of instructions to accomplish the awakening of the processor.